REMARKS

Claims 1-8 are pending, with claims 1, 3, and 7 being independent. Claims 1-5, 7, and 8 have been amended. Support for the amendments may be found in the application at, for example, FIG. 3 and the accompanying text. No new matter has been introduced.

Allowable Subject Matter

Applicant acknowledges with appreciation the Examiner's indication that claims 2, 4, and 8 are directed to allowable subject matter.

Specification

The specification has been objected to for not including a statement claiming priority to Japanese Patent Application No. 2003-373514. The specification has been amended to include such a statement, consistent with the Application Data Sheet submitted when the application was filed. Accordingly, applicant respectfully requests reconsideration and withdrawal of this objection to the specification.

Claim Objections

Claims 1, 2, 3, and 7 has been objected to for various informalities. Claims 1, 3, and 7 have been amended to replace "resisters" with "registers." Claims 1 and 7 have been amended to replace "first logic circuit" with "first logic circuits." Claim 2 has been amended to replace "second logic circuit" with "second logic circuits" and to replace "fourth logic circuits" with "fourth logic circuit." Accordingly, applicant respectfully requests reconsideration and withdrawal of this objection.

Claim Rejections – 35 U.S.C. § 112

Claims 1-8 have been rejected under 35 U.S.C. § 112, second paragraph. Applicant has amended claims 1-5, 7, and 8 to correct grammatical and idiomatic errors. Accordingly, applicant respectfully requests reconsideration and withdrawal of this rejection.

Claim Rejections—35 U.S.C. § 103

Claims 1, 3, 5, 6, and 7 have been rejected under 35 U.S.C. § 103 as being unpatentable over Rajsuman (U.S. Patent No. 6,678,645) in view of Monthie (U.S. Patent No. 7,062,739). Applicant respectfully requests reconsideration and withdrawal of this rejection because neither Rajsuman, Monthie, nor any proper combination of the two describes or suggests all of the features of amended independent claims 1, 3, and 7.

In particular, neither Rajsuman, Monthie, nor any proper combination of the two describes or suggests first logic circuits each including a first group of registers to which external data is written in a first latching step after the external data is input and a first control circuit for controlling the first group of registers, and second logic circuits each including a second group of registers to which the external data is not written in the first latching step and a second control circuit for controlling the second group of registers in accordance with a first output signal from the first logic circuits, as recited in amended independent claim 1.

The Office Action acknowledges that Rajsuman does not disclose a group of registers (*see* Office Action mailed April 16, 2008 at page 4) and, as such, Rajsuman also does not disclose a control circuit for controlling a group of registers. As a result, for these features, the Office Action relies on Monthie.

Monthie discloses a combination of diffused intellectual property (IP) blocks (102) which include registers. *See* Monthie at col. 2, lines 37-44. However, Monthie does not describe or suggest a first control circuit for controlling a first group of registers or a second control circuit for controlling a second group of registers. Nor does the Office Action contend that Monthie does so. Therefore, Monthie, like Rajsuman, does not describe or suggest the noted features of amended independent claim 1.

Moreover, the Office Action has not satisfied its burden of establishing a *prima facie* case of obviousness. The Office Action conclusorily states that "data registers are now commonly used at the I/O interfaces of complex macro/core blocks in order to control the I/O specifications of these blocks for possible integration in an SoC design" in contending that it would have been obvious to one of ordinary skill in the art to combine Rajsuman and Monthie. "[R]ejections on

obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *See* MPEP § 2143.01(IV) (*citing KSR International Co. v. Teleflex Inc.*, 550 U.S. ___, ___, 82 USPQ2d 1385, 1396 (2007) *quoting In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006)) (emphasis added).

Finally, the Office Action is relying on improper hindsight reasoning utilizing the applicant's application. The application, on page 4, line 23 to page 5, line 6, states:

> In the first design step, signals between logic blocks and a part of each logic block are designed. The part of each logic block here means a logic circuit including a register for latching an input data signal transmitted to each logic block firstly and a control circuit for controlling the register. The control circuit also generates control signals serving as other control signals used within each logic block. In the invention, this part is referred to as a first logic circuit whereas other part within the logic block is referred to as a second logic circuit. Further, a group of registers for latching an input data signal transmitted to each logic block firstly is referred to as a first group of registers whereas a group of registers included in the second logic circuit is referred to as a second group of registers.

Therefore, the suggestion that "data registers are now commonly used at the I/O interfaces of complex macro/core blocks in order to control the I/O specifications of these blocks for possible integration in an SoC design," without explicit teaching of such a suggestion, is "knowledge gleaned only from applicant's disclosure" and is, therefore, improper. *See* MPEP § 2145(X)(A).

Accordingly, for at least these reasons, applicant respectfully requests reconsideration and withdrawal of this rejection of amended independent claim 1.

Amended independent claim 3 recites, in part, a first logic circuit including a first group of registers to which external data is written in a first latching step after the external data is input and a first control circuit for controlling the first group of registers, and a second logic circuit including a second group of registers to which the external data is not written in the first latching step and a second control circuit for controlling the second group of registers in accordance with a first output signal from the first logic circuit.

For at least the reasons discussed above in connection with amended independent claim 1, applicant respectfully submits that neither Rajsuman, Monthie, nor any proper combination of the two describes or suggests the noted features of amended independent claim 3 and its dependent claims 5 and 6.

Amended independent claim 7 recites, in part, first logic circuits each including a first group of registers to which external data is written in a first latching step after the external data is input and a first control circuit for controlling the first group of registers, and second logic circuits each including a second group of registers to which the external data is not written in the first latching step and a second control circuit for controlling the second group of registers in accordance with a first output signal from the first logic circuits.

For at least the reasons discussed above in connection with amended independent claim 1, applicant respectfully submits that neither Rajsuman, Monthie, nor any proper combination of the two describes or suggests the noted features of amended independent claim 7.

Conclusion

Applicant respectfully submits that all claims are in condition for allowance.

It is believed that all of the pending issues have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this reply should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this reply, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

The fee in the amount of $120 in payment of a one-month extension of time fee is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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